LNA Project Report

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RF2
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Introduction

The goal for our project was to design, fabricate and test a low noise amplifier with the specific criteria listed below on Table 1. A low Noise amplifier is an amplifier that while providing a significant amplification of the incoming signal while also providing very little noise. This can be accomplished by designing the BJT to operate with a specific bias and being well matched. This document show my design from beginning to end.

Project Goals

Specifications	Design #2 Goals	Simulated	Measured
Board Type	FR4	FR4	FR4
Fc (GHz)	1.4	1.4	1.4
%BW	15	128	None
Gain (dB)	15 +/- 1	15.282	6.748
NF Max (dB)	1.5	1.386	Not Measured
Input RL (dB)	>10	7.783	20.748
Output RL (dB)	>10	16.996	1.52
Stability	Unconditional	Unconditional	Not Measured
Z0 (Ohms)	50	50	50

Table 1: Design specifications

Design

I began the design process by doing a stability analysis shown in figures 1-3. The goal was to pick the appropriate biasing point in which will allow the transistor to be unconditionally stable between the frequencies of 1.2GHz and 1.4GHz. The optimum Ibb condition for the target frequency of 1.4 GHz turns out to be 50uA. This allows K>1, |Δ|<1, and B>0 which is the indication that the transistor will be unconditionally stable at 1.4GHz.

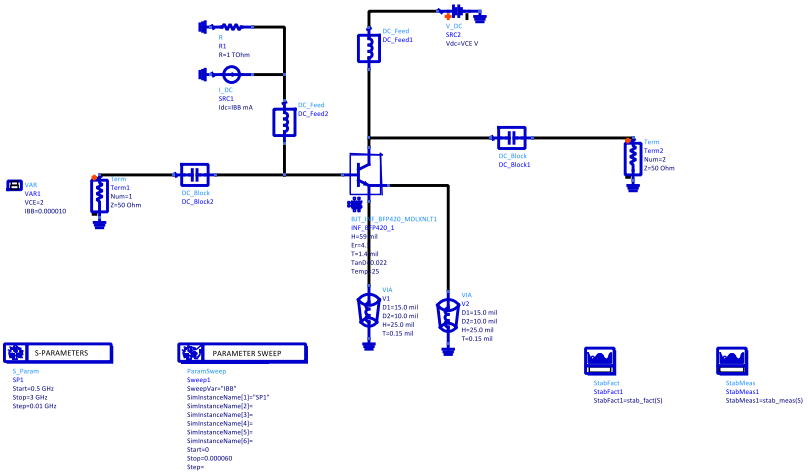

Figure 1: Stability testing circuit

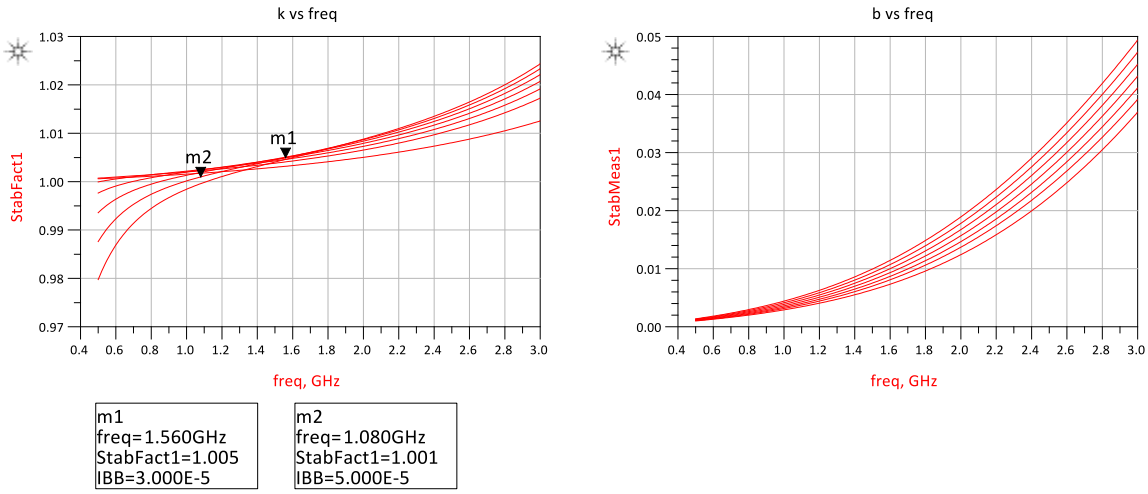

Figure 2: Sweeping Ibb while measuring K (left) and B(Right)

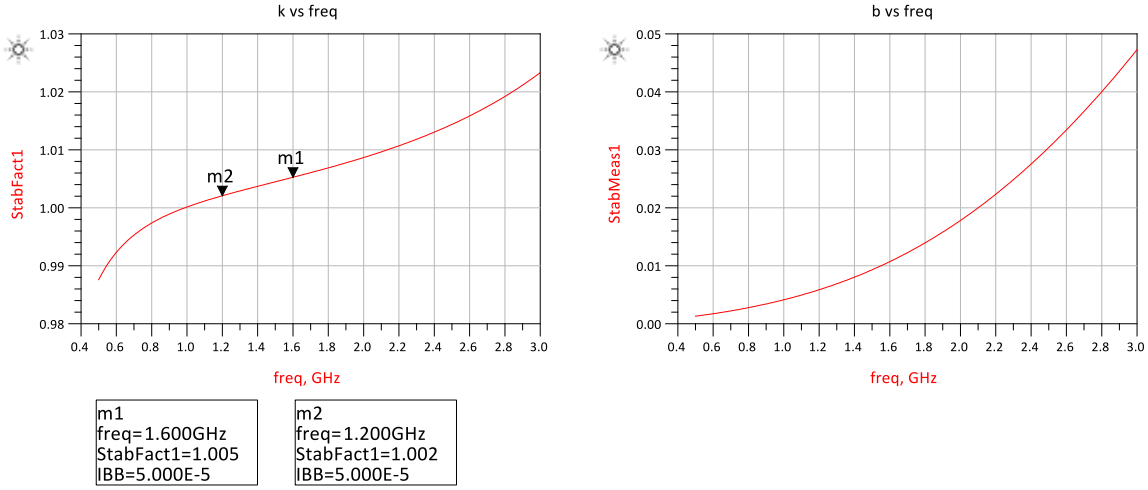

Figure 3 : Target Ibb current picked to be 50uA

Once the proper biasing for base was picked I was able to move towards designing the both the input and output matching networks. The first step is to find the S parameters at the specific biasing point in which I am using. This was found to be 50uA, and a VCE that is equal to 3v. Noise circles and Ga circles can be overlapped as shown in figure 4 below. The overlapping optimal noise and gain location for Γs can be seen where the 1.5dB noise circle overlaps the gain circles. For 50uA the gain circles are very small and overlap the 1.5dB noise circle perfectly. The input impedance was chosen to be equal to **26.401+j22.006.**

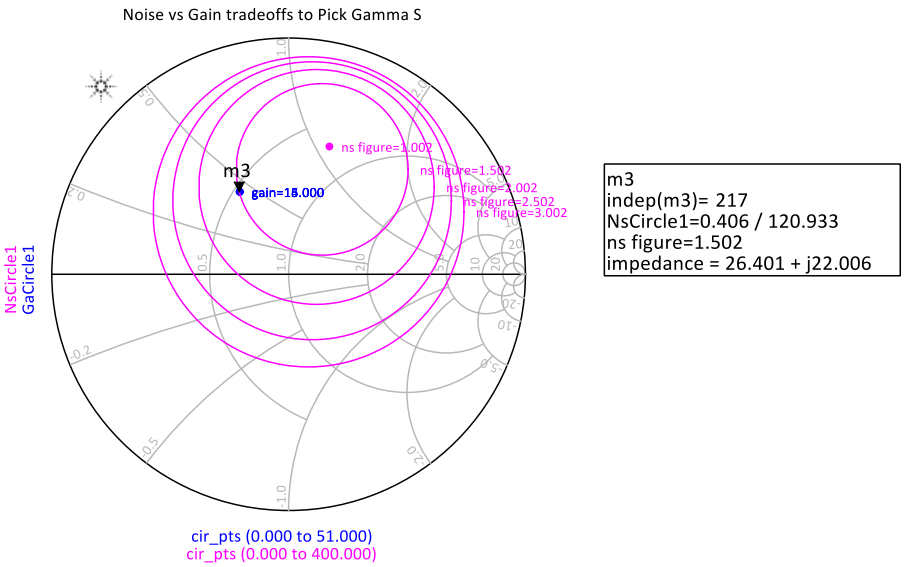

Figure 4: Noise circles and Ga circles for biasing of Ibb=50uA and VCE=3v

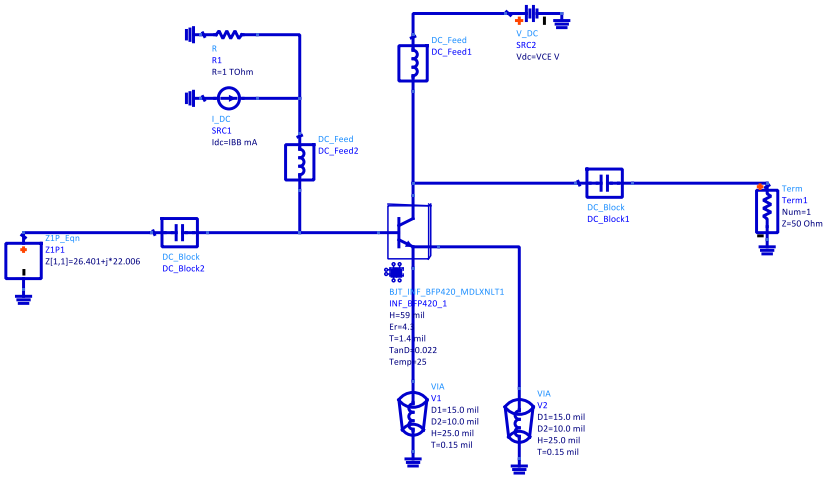

Figure5: Gamma S has been chosen in order to pick Gamma L

The optimal Γs was put in the circuit shown in Figure 5. S11 was then measured in order to determine what Γout is shown in Figure 6. From Γout I was then able to choose the optimal Γl which was the conjugate of Γout.

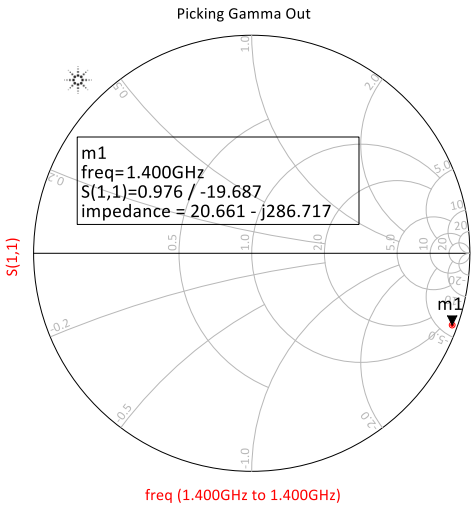

Figure 6: Γout shown after picking the appropriate Γs

After determining the input impedance needed to have the desired gamma S the components were picked and optimized as shown below in figures 7, 8, and 9. The optimal components ended up being a series **C=38.4748 pF, and a shunt L=6.01209 nH.**

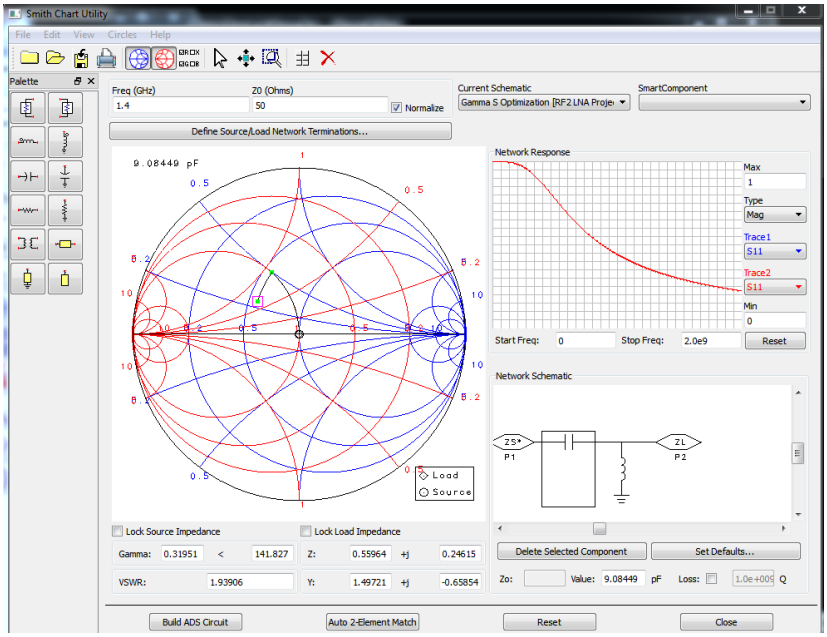

Figure 7: Picked L=6.40785nH, and C=9.08449 using the Smith Chart Tool

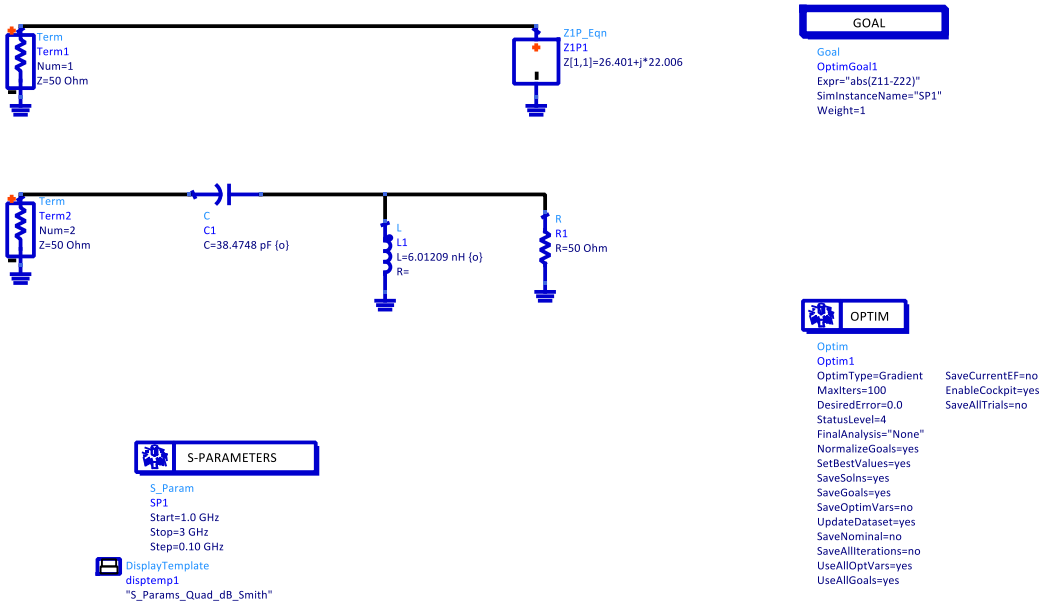

Figure 8: Post Optimization of Γs components

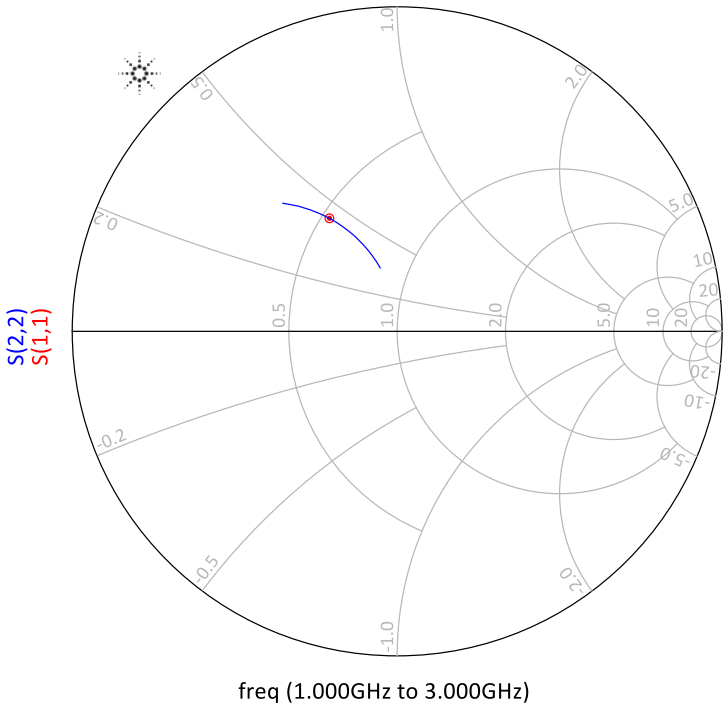

Figure 9: Optimized Gamma S matching components

The Γl was chosen based upon the Γout values that were picked. The Γl is the conjugate of Γout. The load impedance was chosen to be **20.661+j286.717.** Components were selected based up on the smith chart (Figure 10), **Shunt L= 7.43102nH, and Series L= 26.51252 nH.**

Once a DC blocking capacitor was added, optimization was then completed shown in figures 11 and 12. Components values were then placed in the circuit along with the input matching network and then optimized. The final input and output matching networks are shown in figure 13, and S11 and S22 shown in Figure 14.

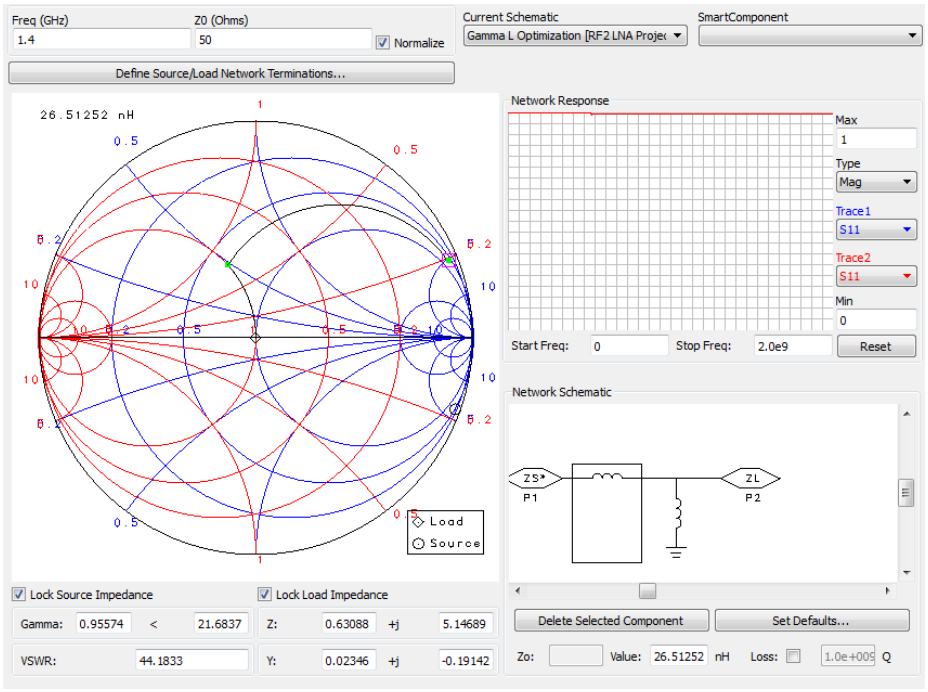

Figure 10: Picking Output impedance matching network components

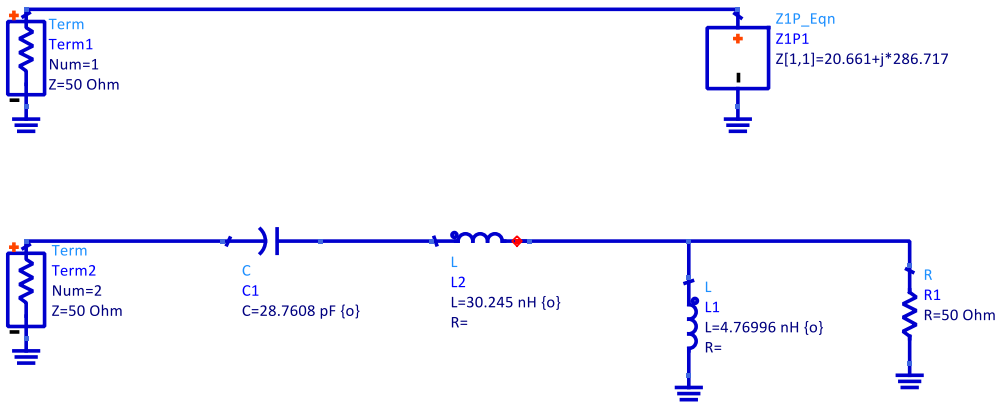

Figure 11: Post optimization components for output impedance matching network

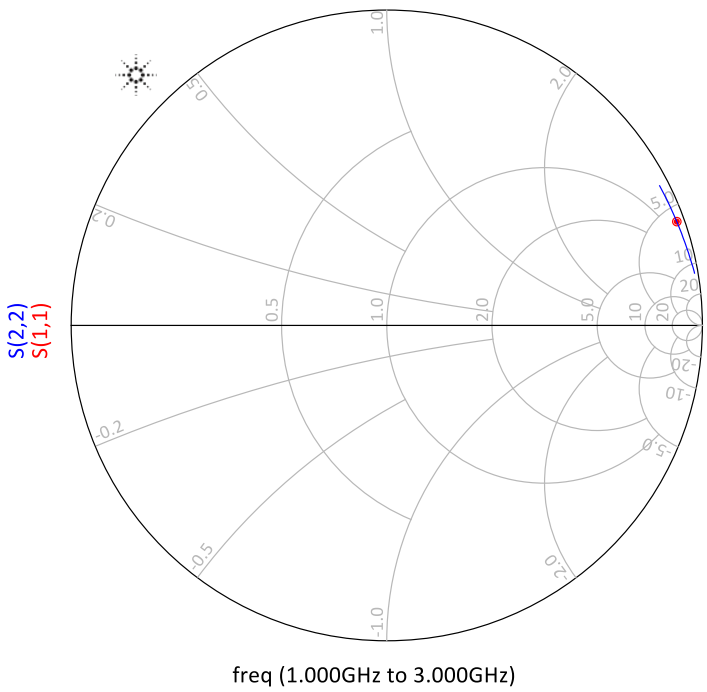

Figure 12: Post optimization components for output impedance matching network

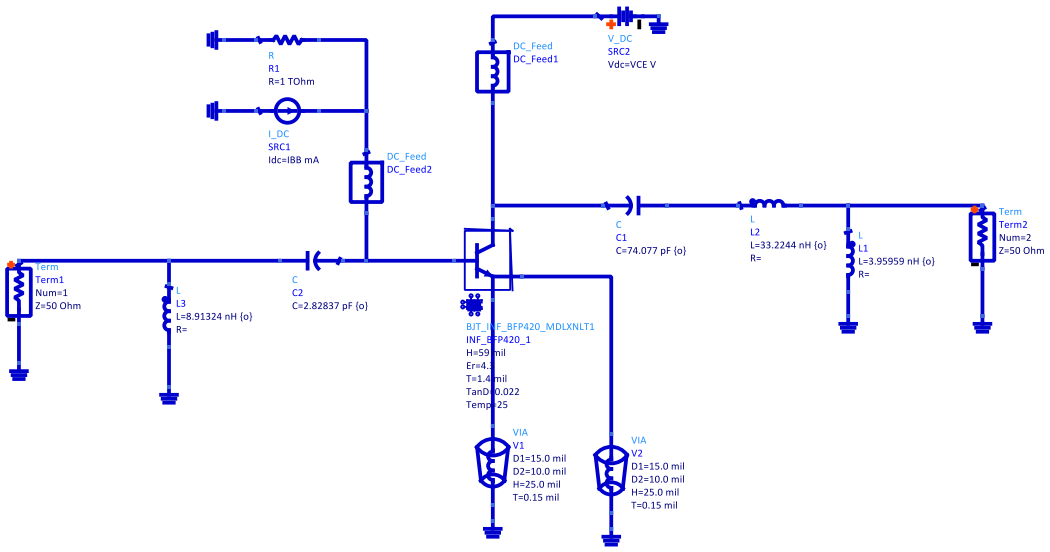

Figure13: Final Input and output matching networks post optimization Ibb= 50uA, and VCE = 3v

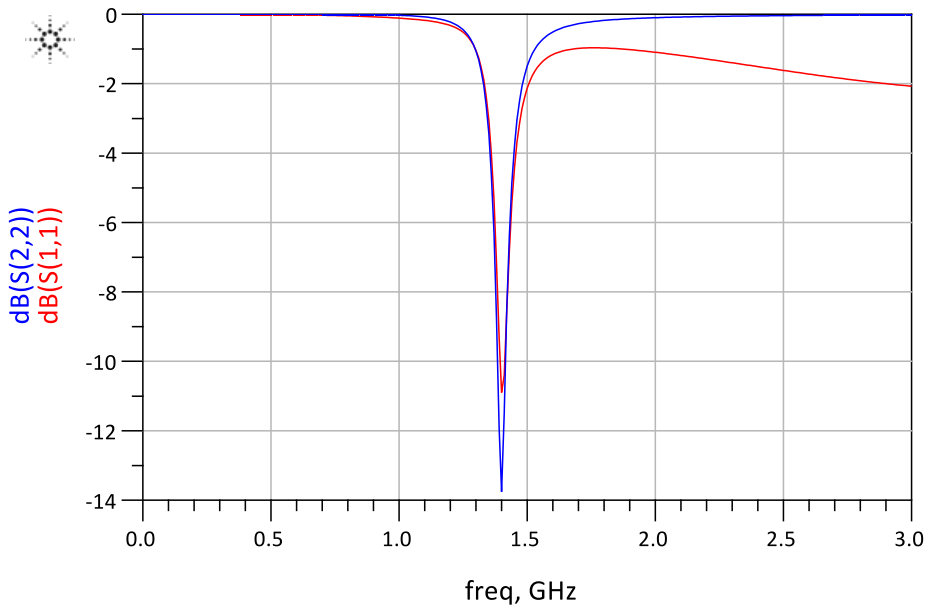

Figure 14: S11 and S22 with input and output matching networks added

Once I added all of the RF chokes as well as capacitors to ground to try to reduce the AC going to the source the circuit needed to be optimized even more. Figure 15 shows the final design including all the bias components of the circuit. Simulated data is shown in figure 16.

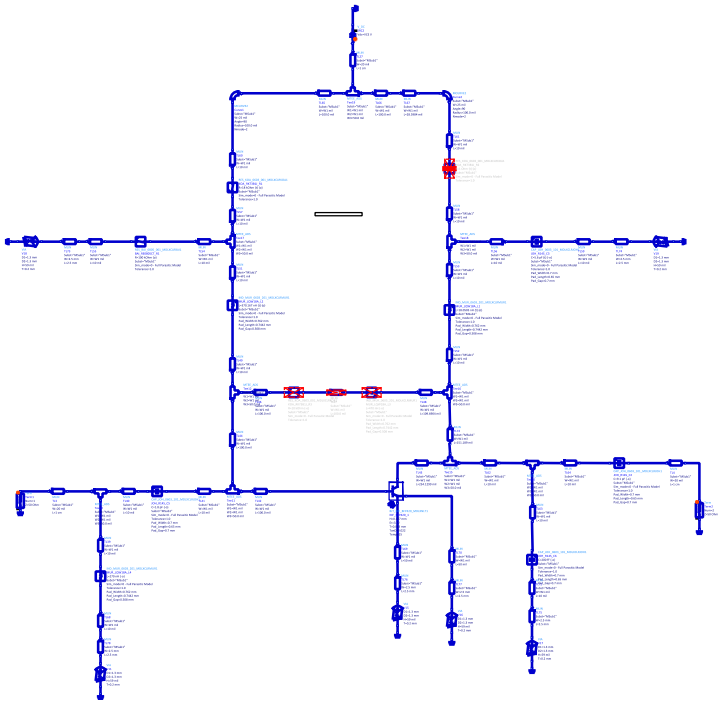

Figure 15: Schematic of our fabricated design

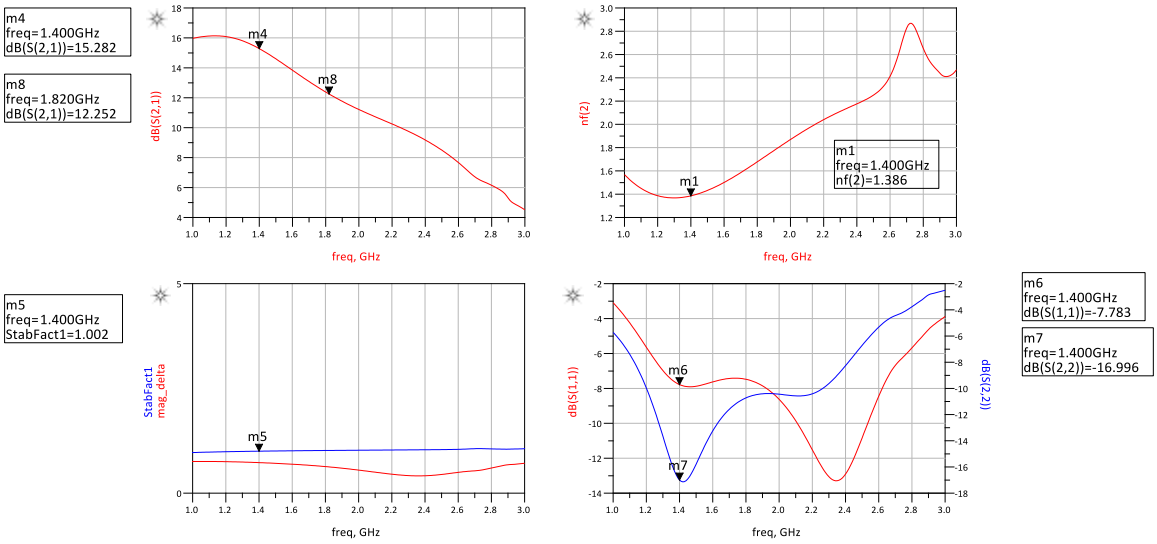

Figure 16: Circuit Simulated Values prior to fabrication

Fabrication and Testing

The design was then fabricated using a LPKF S62 milling machine in order to realize the layout shown below in figure 17. The final board soldered together is shown in figure 18. The Vias were filled and soldered with copper wire and the BJT was missing pads which ended up needing to soldered across with bridges to fill the void. These two components contributed to the measurement not being as well as it could have been. Figure 19 shows the simulated data versus the measured data. The S11 follows rather well comparatively, but the others are not in as good agreement due to the before mentioned problems.

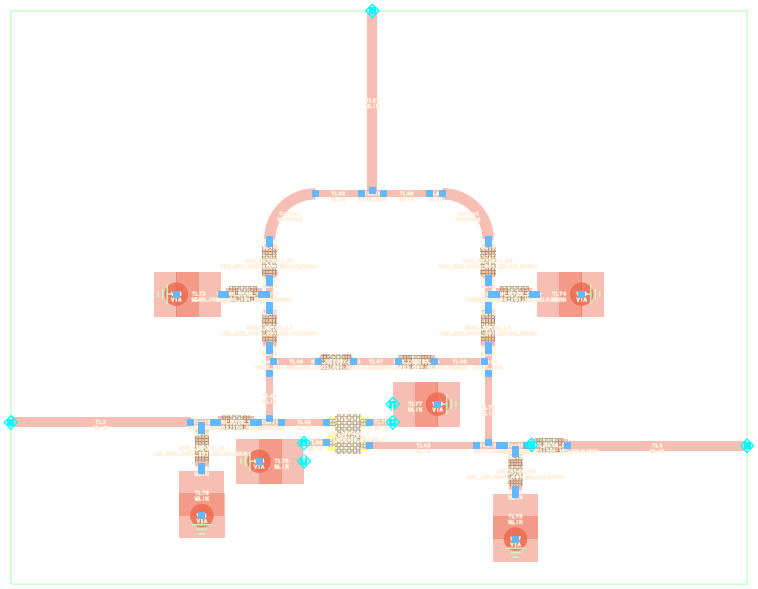

Figure 17: Layout of the fabricated LNA design

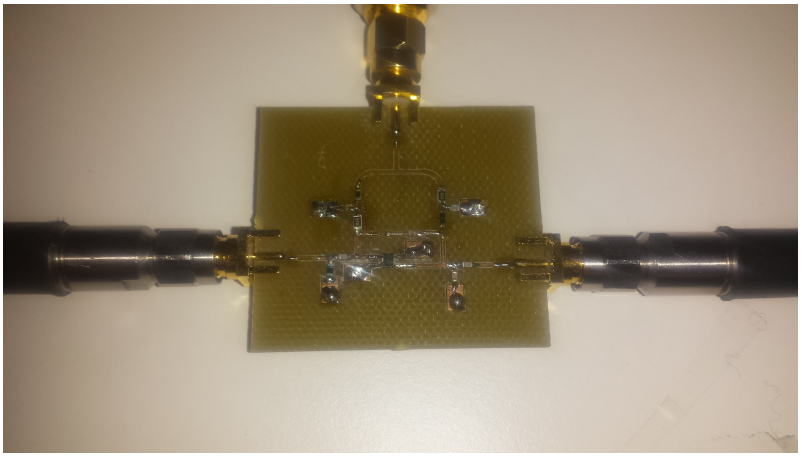

Figure 18: Fabricated LNA on FR4

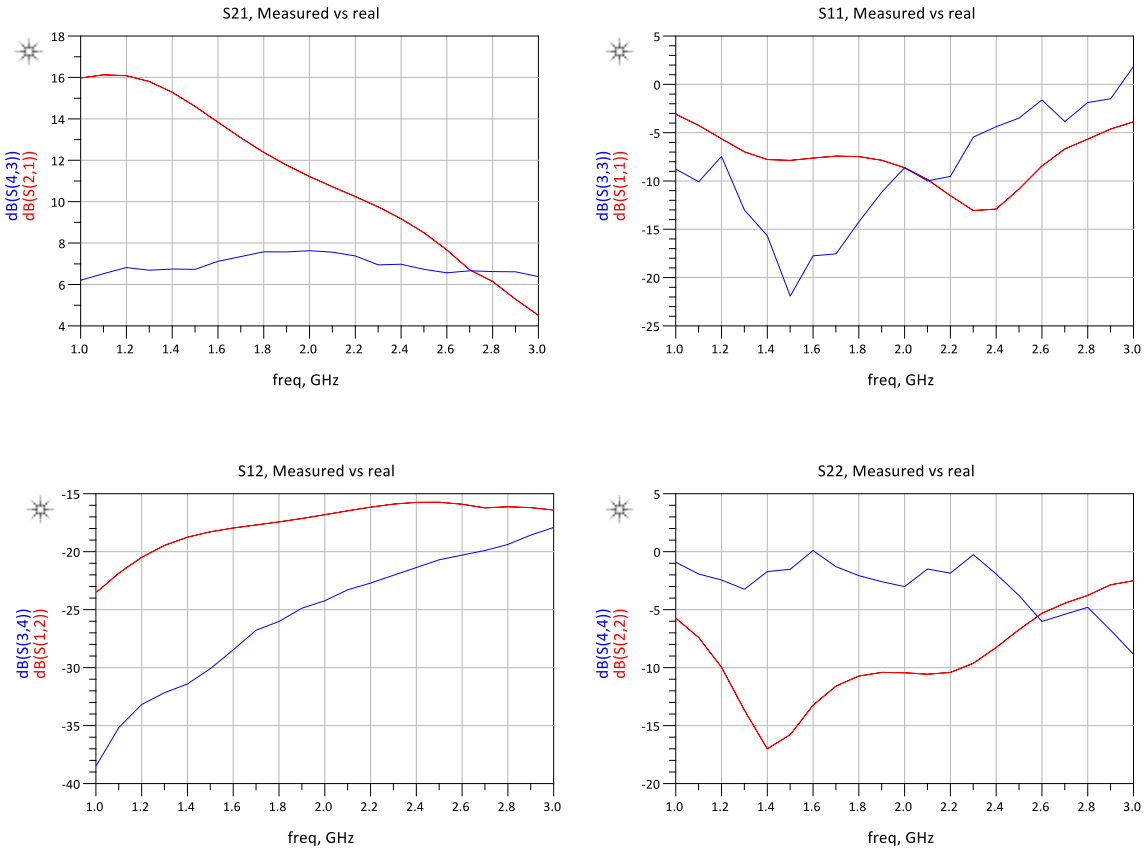

Figure 19: Simulation vs measurements of our fabricated design

Conclusion

A Low Noise Amplifier with the center frequency of 1.4GHz and the design specs listed in Table 1 was designed, fabricated and tested. In the end the measured results showed that there was alot of parasitics in the circuit that contributed to poor matching which caused the simulated and measured data to be different than one another. Also contributing to the losses are the missing BJT pads during the fabrication step. In the end the design was realized by fabrication and testing. Gain turned out to be low, but the biasing for the BJT was measured to be close to 0.7v which helped to produce the low amplification of 7.5dB. This was lower than that was expected during the design process, but still amplification that was measurable.