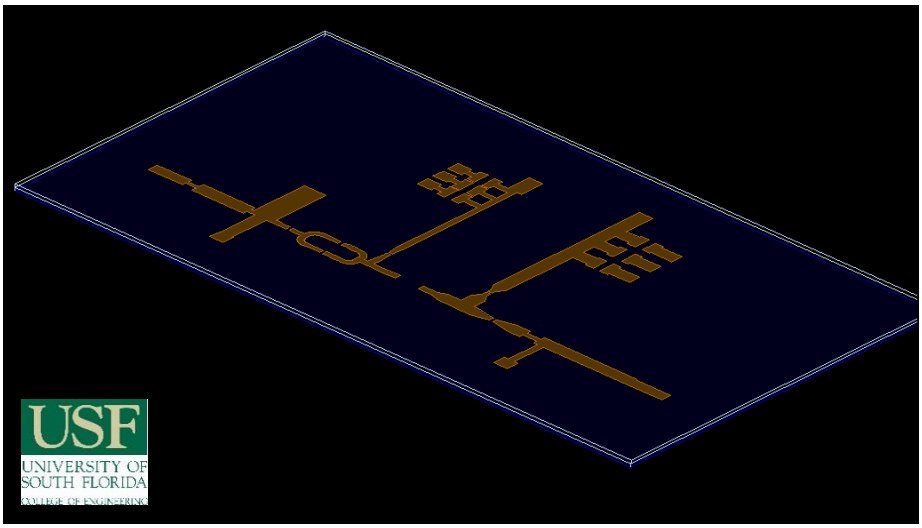
University of South Florida

College of Engineering

Electrical Engineering, MSEE Program



EEE 6368: RF and Microwave Power Amplifier Design

Design of a 30 W Power Amplifier utilizing a Qorvo T2G6003028-FL GaN HEMT device

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Abstract

A Power Amplifier centered at 2.8 GHz utilizing a Qorvo T2G6003028-FL Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) has been designed and simulated for future fabrication on a 3.5”x3.75” Rogers 4305B board. It has a maximum Power Added Efficiency (PAE) of 63%, and output power of 45 dBm when the input power is 37 dBm. In this report the design process of this amplifier is summarized from beginning to end and simulated results are shown.

Introduction

The goal of this design project was to design a Power Amplifier centered at 2.8 GHz that can achieve the design specifications shown below in ***Table 1: Target Specifications***. It is biased as a class AB amplifier in order to obtain a minimum of PAE of 55%. The simulation program that I used to do the design was Keysight Advanced Design System (ADS) utilizing the Modelithics library for component models.

Amplifier Type	Class AB High Power amplifier
Device Type	Qorvo T2G6003028-FL
Center Frequency (GHz)	2.8
Bandwidth (%)	20
Gain	10 dB with +/- flat across the band
Power added Efficiency (%)	>55
Min Power (dBm)	43.5
Min PAE Goal (%)	50
Input Return Loss (dB)	>10
Board type	Rogers 4350B (Er=3.75), 20mils thick, 1E cladding

Table 1: Target Specifications

Design Method/Calculations

Finding the Biasing Point

The first step taken in the design process was to select the appropriate biasing point for my device. According the to manufacturer’s datasheet 28v for V_{ds} and ~200mA for I_{ds} was a good condition to bias for Class AB. In order to get the corresponding current level needed I ended up using a bias of -3v for the V_{gs} which gave me 230 mA based upon my simulation which is ideal for the Class AB condition.

Stabilization

Next I added a network of a parallel R and C to the input in order to stabilize the circuit. This was necessary, but also brought down the gain considerably once added. The factors that were needed to be checked for all frequencies from 1 MHz to 6 GHz (Upper range of the device) to ensure stability are shown below in ***Table 2: Stability considerations from 1 MHz to 6 GHz***. If any one of these are not addressed during the design stages the circuit could oscillate once fabricated. Capacitator banks were also added next to both sources as well in order to help even more with the stabilization. Values of 1000

Stability factor or k	>1
Delta	<1
b	>0
dB(S21) at 1MHz only	<0

Table 2: Stability considerations from 1 MHz to 6 GHz

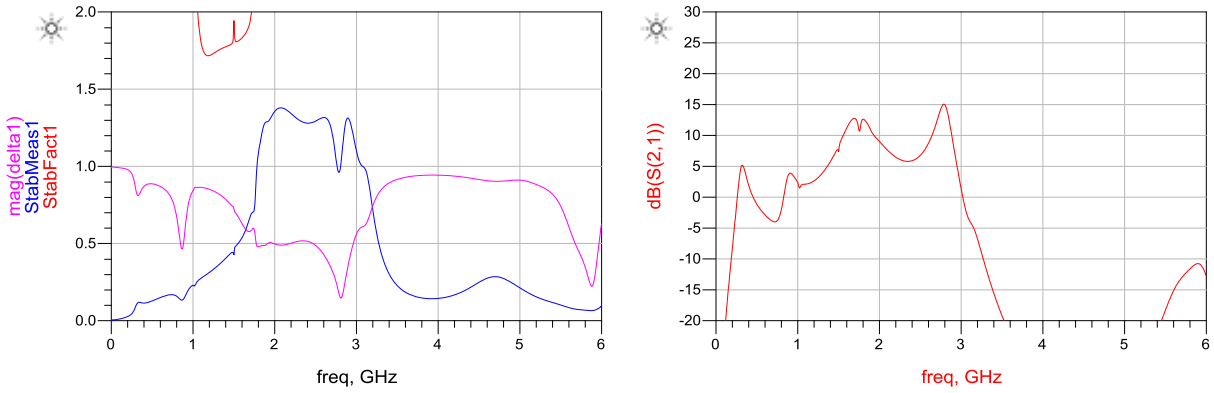

Figure 1: Stability design parameters (1MHz - 6 GHz)

Input Matching Network

For the matching network on the input the goal for my design match it well enough to have the input return loss at 2.8GHz to be less than 10dB, while at the same time providing the widest bandwidth that I can possibly achieve. Parallel shorted and open stubs have been utilized to attempt to provide a wider bandwidth match [1]. The goal was is to wrap the frequencies above and below my center frequency towards the center of the smith chart to get a wider match.

One aspect of the matching network that was decreasing the gain of the circuit at first was the size of DC blocking capacitors that I chose to use. 24pF where chosen to start for both the input and the output caps, but due to my resonant frequency being at 2.8 GHz there ended up being Series resonance that was bringing my gain down to 8dB when the goal was to be above 10dB. Below in *Figure 3: Series Resonance effect on Gain* it can clearly be seen that the 24pF ATC 800B cap was decreasing my resonant

frequency. A 100pF ATC 600s capacitor was chosen as a replacement and the gain was able to come above 15dB on the final design.

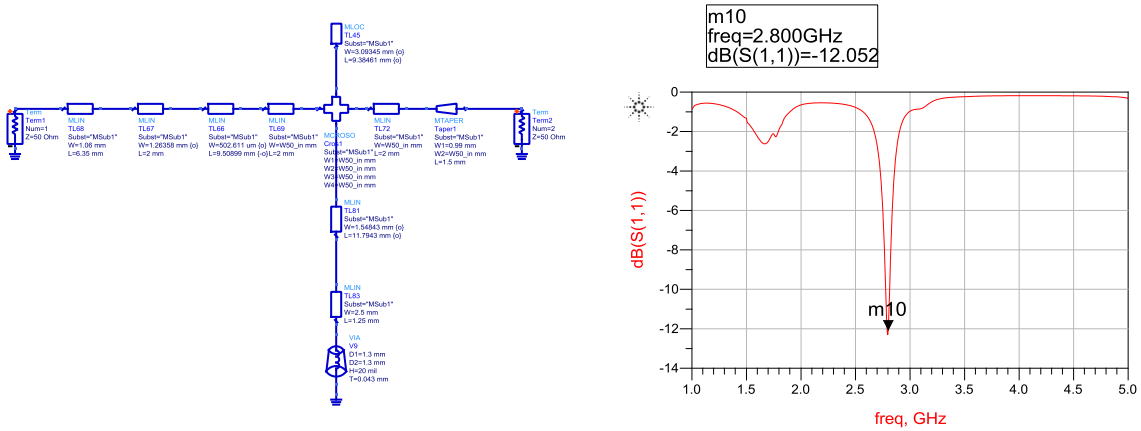

Figure 2: Input Matching Network and S11 when combined with circuit

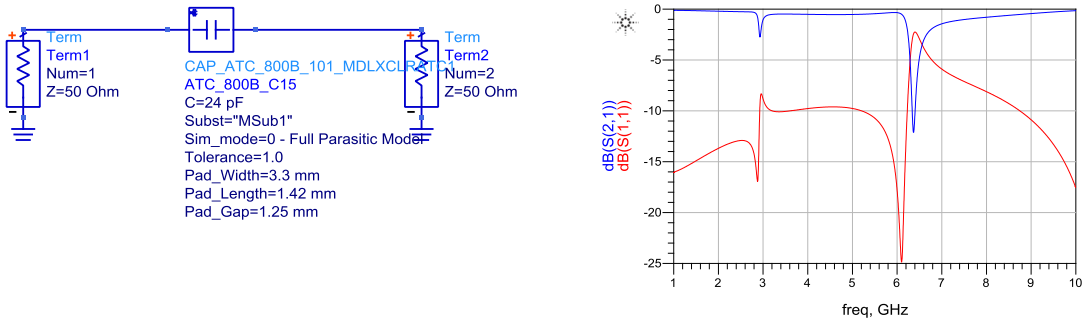

Figure 3: Series Resonance effect on Gain

Output Matching Network

After the I/M (Input Matching) network was added the last step in finalizing the design was to find the optimal load in order to optimize the output power output and PAE needed to meet the requirements for the design as shown in ***Table 1: Target Specifications***. In order to do that a load pull was performed in order to find the correct load needed. For the load pull the input power selected to be used was based upon the P2dB point of the circuit which was found to be 37dBm. Many different loads were shown to the output of the circuit and with each load given the PAE and power delivered were recorded shown in ***Figure 4: Load Pull of circuit***. The load was then selected based upon the requirements for performance outlined in ***Table 1: Target Specifications***. A shorted stub and series transmission line were used to make the load with the corresponding S parameters are shown in ***Figure 5: Output Matching Network and S parameters***. The resulting target and designed values used in the final design are outlined below in ***Table 3: Input and Output impedances***.

	Target Value	Final Design
Zs (R+j*X) ohms	1.865+j*1.005	3.733+j*1.677
Zload (R+j*X) ohms	10.768+j*22.627	14.998+j*28.464

Table 3: Input and Output impedances

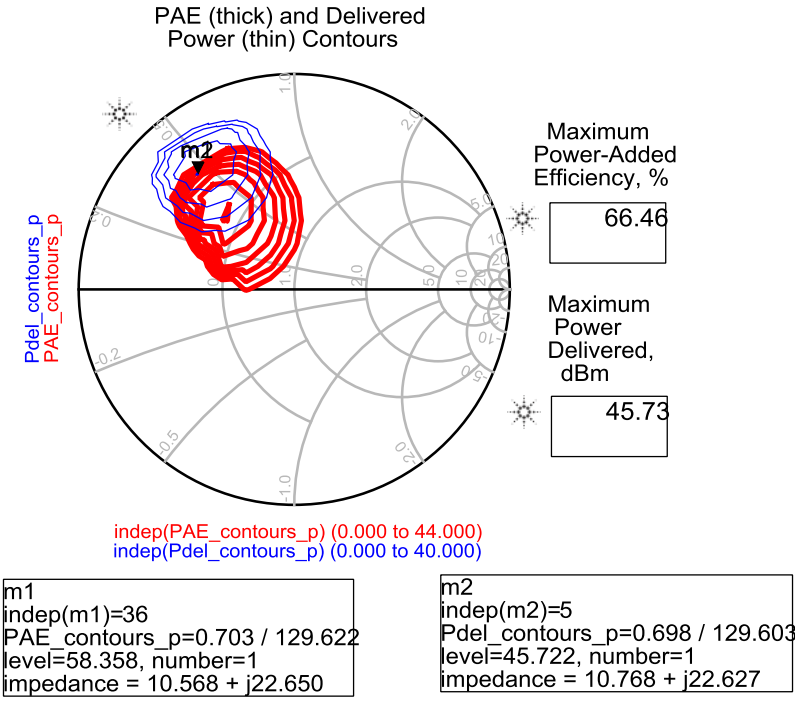

Figure 4: Load Pull of circuit

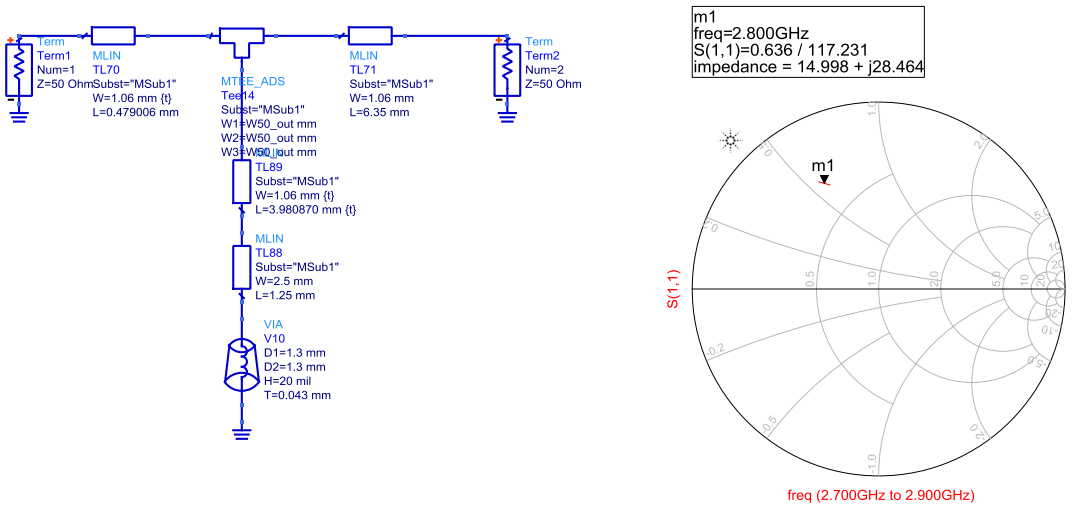

Figure 5: Output Matching Network and S parameters

Design Description

The final schematic is shown below along with component values as well as the complete layout.

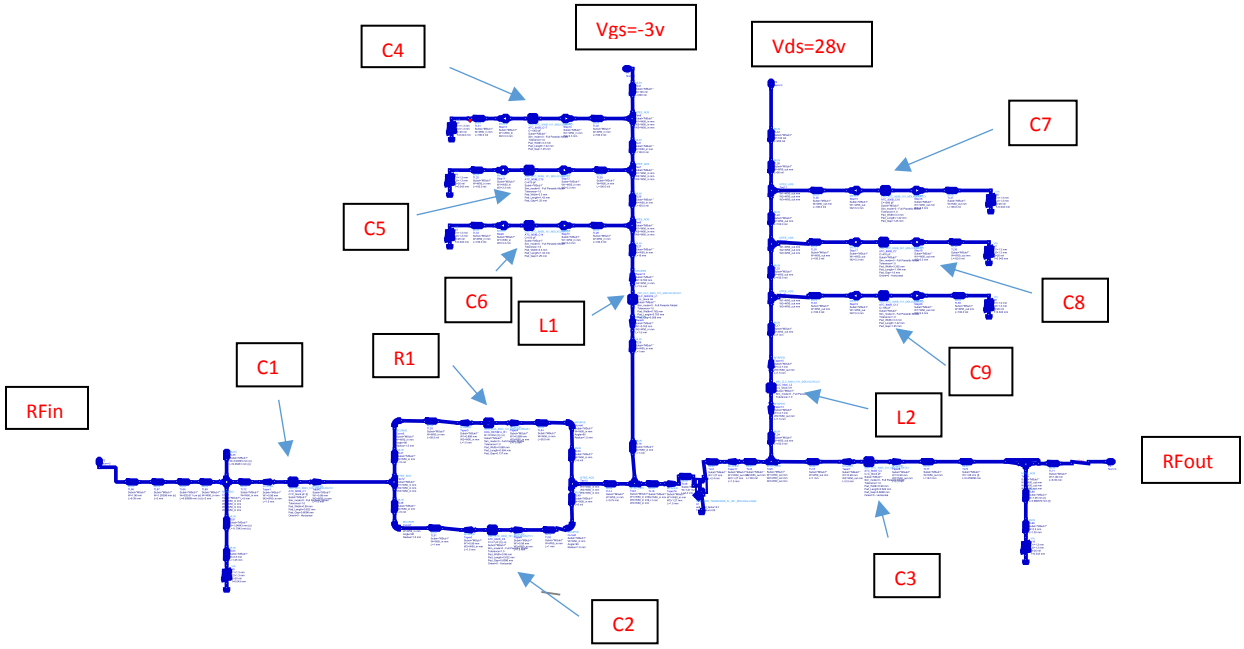

Figure 4: Schematic of circuit

	Type	Component	Value

DC Blocking Caps (x2)	ATC 600s	C1, C3	100 pF
RF Blocking Inductor - Input	Coilcraft 0603CS	L1	200 nH
RF Blocking Inductor - Output	Coilcraft Maxi	L2	200 nH
Stabilization circuit Resistor	KOA RK73B1J	R1	10 Ω
Stabilization circuit Capacitor	ATC 600s	C2	4.7 pF
Source Capacitor banks (x2)	ATC 800B	C4, C7	1000 pF
Source Capacitor banks (x2)	ATC 800B	C5, C8	470 pF
Source Capacitor banks (x2)	ATC 800B	C6, C9	100 pF

Table 4: Schematic Component Values

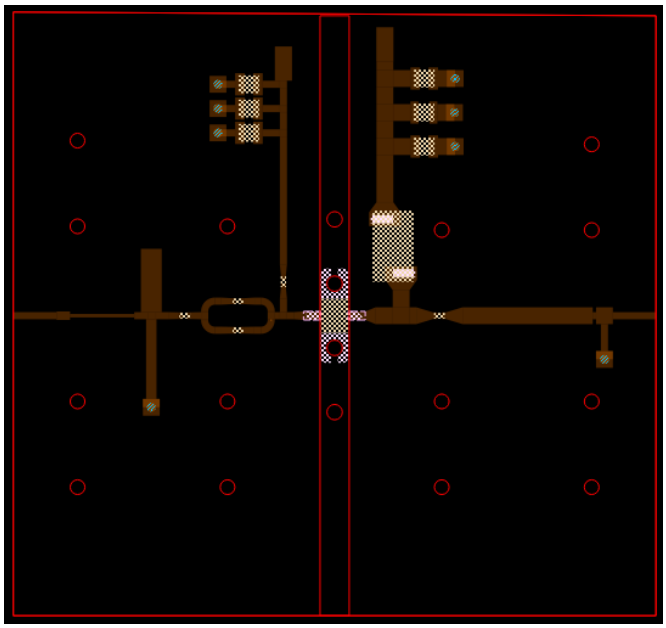

Figure 5: Circuit Layout

Simulation results

	Goal	**Simulation**
Center Frequency (GHz)	2.8	2.8
Gain (dB)	10	14.9
Power added Efficiency (%)	>55	64.3
Min Power (dBm)	43.5	45.2
Input Return Loss (dB)	>10	12

Table 5: Design results

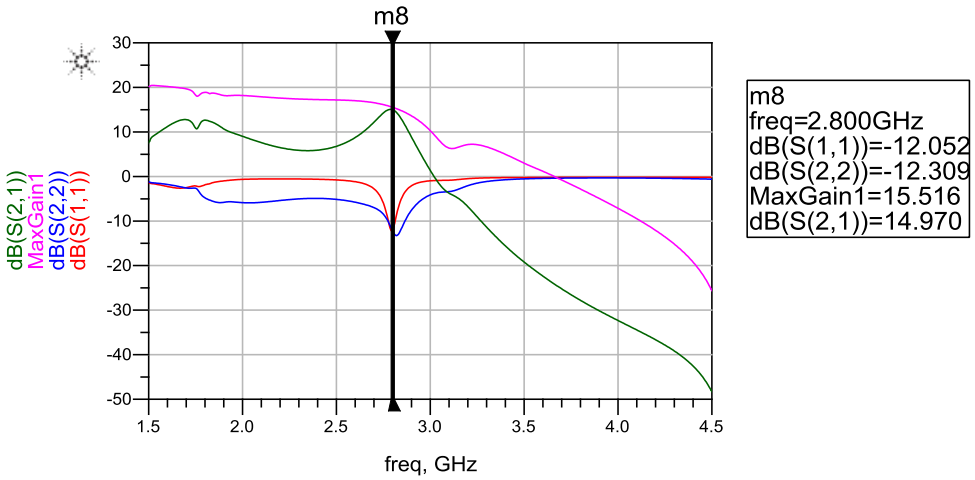

Figure 6: MaxGain, Gain, Input RL, Output RL

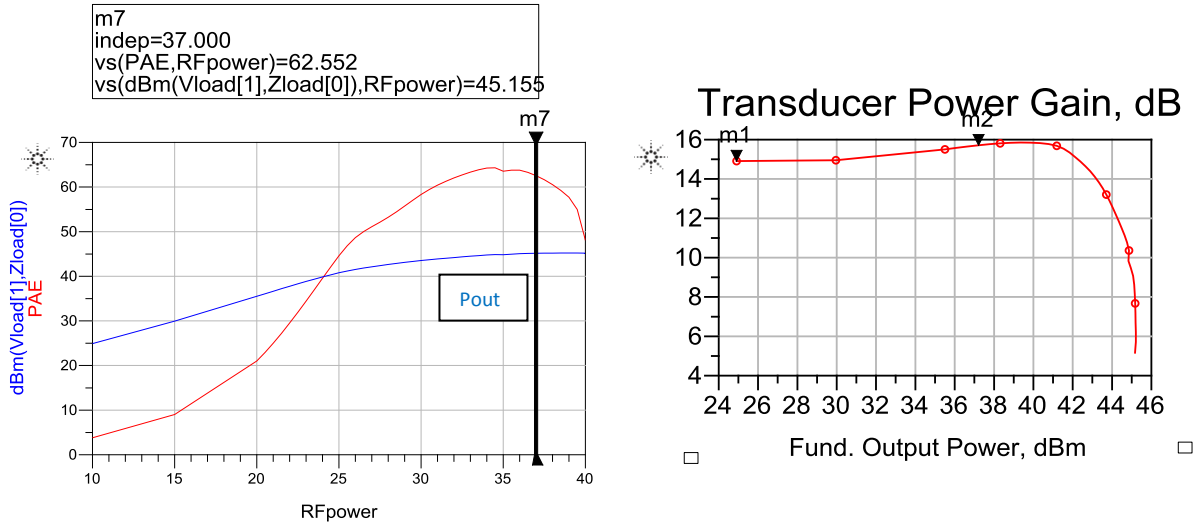

Figure 7: PAE and Pout and Transducer Power Gain

Conclusions

A Class AB Power amplifier utilizing a Qorvo T2G6003028-FL GaN HEMT was designed and simulated. Modeled results show that it the circuit is capable of reaching a PAE of 62.5%, while putting out 45dB of power which meats the design criteria very well. Fabrication and measured results will be following shortly once fabricated next semester. Recommendations for future design updates would be to increase the bandwidth. The input matching network can be modified to get a wider bandwidth.

Bibliography

[1] G. D. Vendelin, Microwave circuit design using Linear and Nonlinear Techniques, Hoboken, NJ: Wiley, 2005.

[2] S. Cripps, Power Amplifiers for wireless communications, Norwood, MA: Artech House, 2006.

[3] V. P. e. al, "High Linearity and high efficency of calss B power amplifiers in GaN HEMT technology," *IEEE Microwave Transactions on Microwave Theory and Techniques,* vol. 21, no. 2, pp. 643-652, 2003.