MMIC Project Report

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MMIC Design
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Abstract

A broadband distributed amplifier has been designed and simulated for the specific purpose of being able to amplify a wide range of frequencies from 2-20 GHz. Broadband amplifiers are very desirable due to the fact that they are very versatile and can amplify a very wide Bandwidth. The desired goals are low noise, and high gain while maintaining a P1dB of 15dBm or greater as shown in table 1. The design and simulation results of this distributed amplifier design are discussed.

Introduction

The goal for this project was to design and simulate a broadband distributed amplifier. The theory of a distributed amplifier is very well know in the theory has been studied for decades. The travelling wave amplifier is one that incorporates transmission line theory in order to gain a wide bandwidth.

Specifications	**Goals**	**Simulated - Ideal**	**Simulated - Real**
Substrate	GaAs	GaAs	GaAs
Freq (GHz)	2-20	2-20	2-20
Gain (dB)	10 +/- 1	>10	>7
NF Max (dB)	4.0	8	12
NF Min Midband (dB)	3.5	3.5	3.5
P1dB min (dBm)	>15 (17 Better)	17	15
VSWR (in)	2.0:1	2.0:1	2.8:1
VSWR (Out)	2.0:1	2.0:1	3.3:1
Supply voltage (v)	3.5	3.5	3.5

Table 1: Design specifications

$$Z_0 = \sqrt{\frac{L_g}{C_{gs}}} \quad (1)$$

$$f_c = \frac{1}{\pi\sqrt{LC}} \quad (2)$$

$$C_{add} = C_{gs} - C_{ds} \quad (3)$$

$$gain = -ng_m = \frac{1}{2}ng_m Z_0 \quad (4)$$

$$n\omega^2 C_{gs}^2 R_i Z_0 \ll 1 \quad (5)$$

Design Procedure

I began the design process by first using a model of the enhancement mode transistor to find out the values of Cgs, Cgd, ri, gm, Cds, and Rds that will be inherent in the transistor. By setting up and simulating the transistor with the desired finger width of 26um and 4 fingers per transistor I was able to get the desired parameters at 10GHz which is midband to the frequency range in which I desire to amplify.

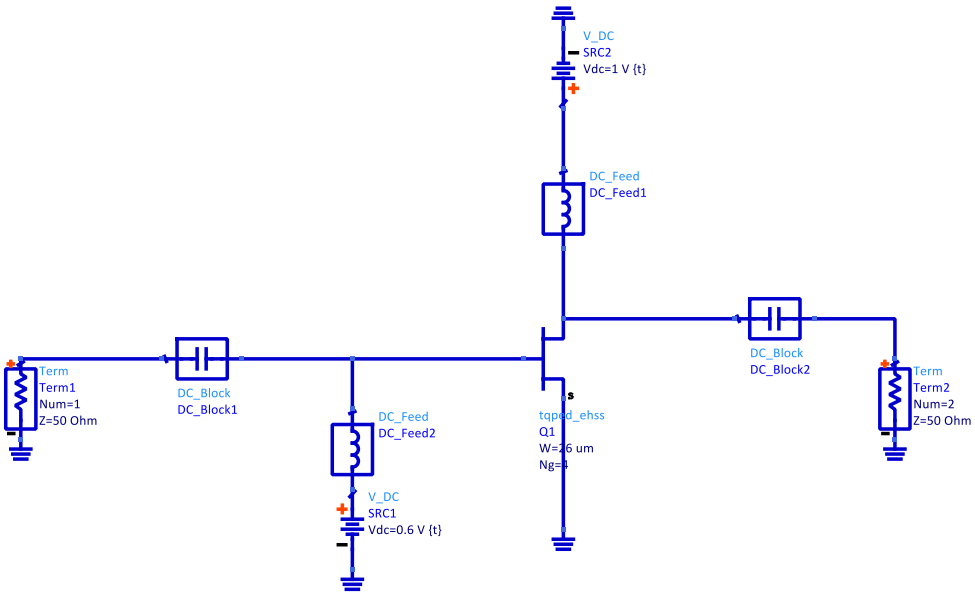


Figure 1: Transistor small signal parameters circuit

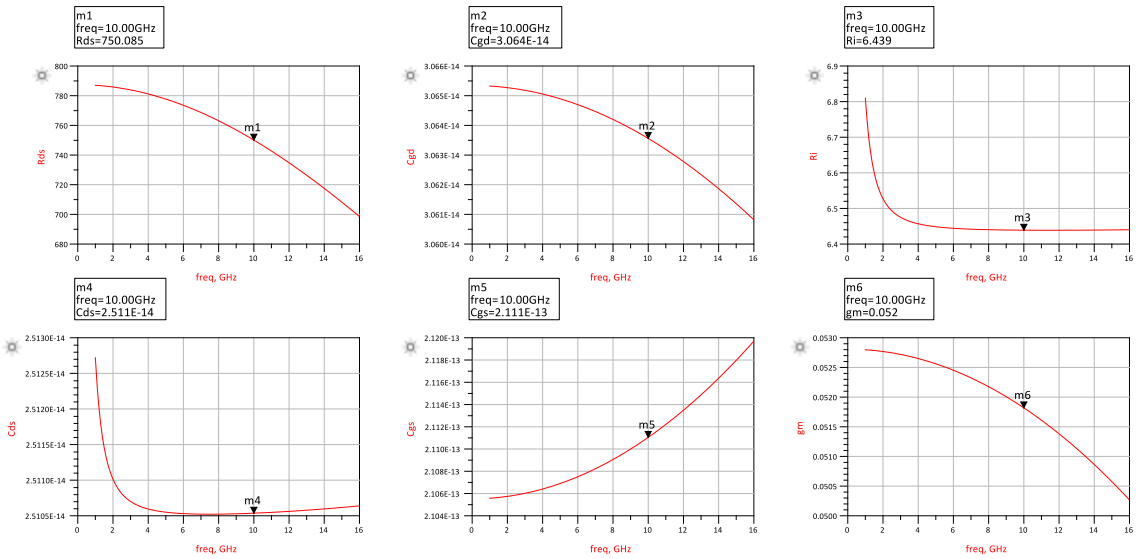


Figure 2: Transistor small signal parameter values

I then used the extracted Cgs and Ri values to determine the maximum number of sections I can use by using equation 5, then I found my cutoff frequency using equation 2, and gm was then calculated using equation 4.

Fingers= 4	Cgs = 0.2pF	Ri = 6.439Ω
Finger Width= 26um	n = 5	Lg = 0.5nF
Fc = 1THz	Gm=0.052	Cadd=0.186nH

Table 2: Calculated values for circuit components

With these values I used them to set up my ideal design with 5 stages, and I was able to design and simulate a 5 Stage amplifier using ideal components.

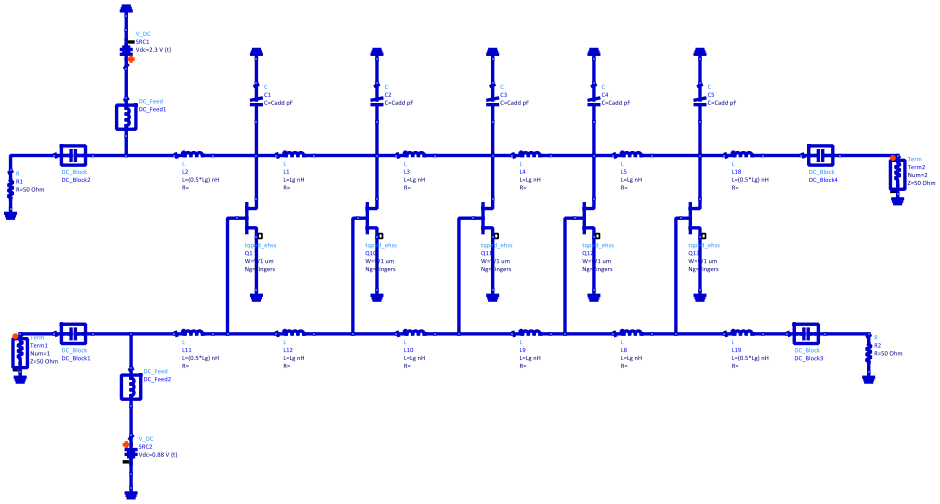


Figure 3: Ideal 5 stage Distributed amplifier

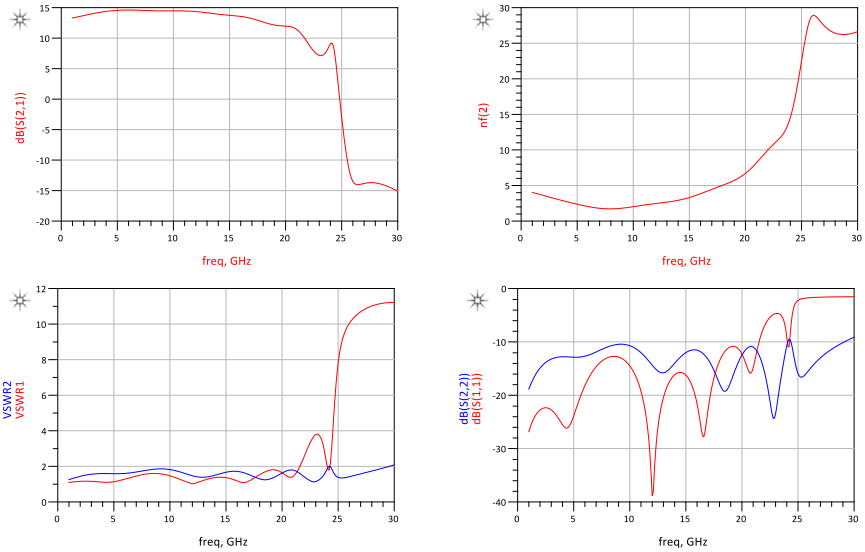
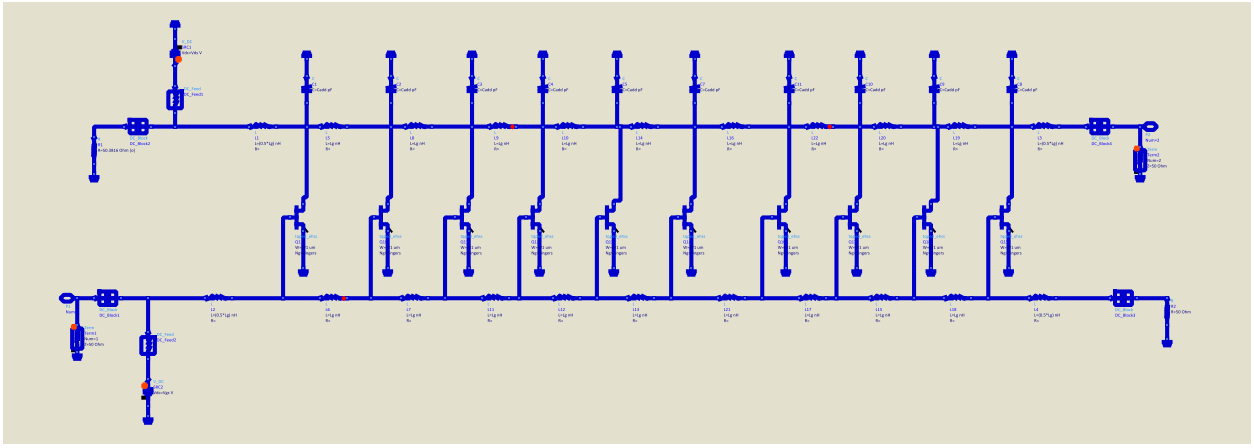


Figure 4: Ideal 5 stage Distributed amplifier Simulation

I Just to see what would happen if I extended the design out to 10 stages I connected and tested the 10 stage amplifier below. The design had better bandwidth and higher gain than with 5 stages, however once realized to the real design it proved to not be as good as the original design with 5 stages.



Var Eqn
VAR
VAR1
Lg=0.780953 nH
Vgs=0.8 V
Vds=3.5 V
Fingers=2
W1=25 um
Cadd=0.124769 pF

Figure 5: Ideal 10 stage Distributed amplifier

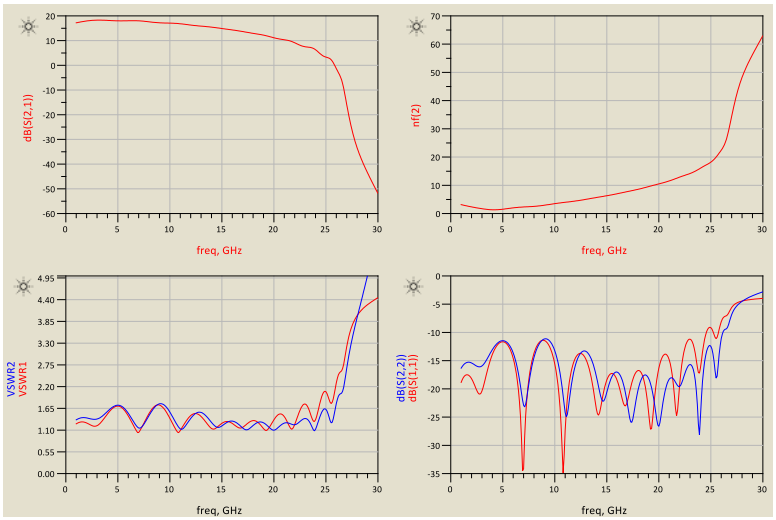


Figure 6: Ideal 5 stage Distributed amplifier simulation

Adjusting the P1dB point for this design project was a challenge. In order to get a good P1dB of 15dBm or greater the most critical aspects of the design were the finger width, number of fingers, and Vds. Below in figure 7 is a plot of my P1dB measured during the ideal simulation. Translating the same P1dB to the real design required some optimization and tweaking of the design parameters.

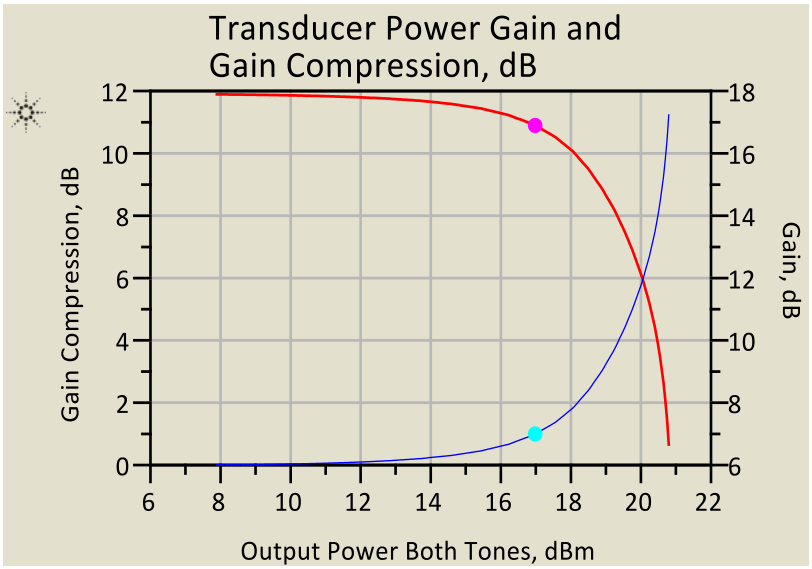


Figure 7: Simulated P1dB - Ideal design

Schematic and Layout

Once I simulated my ideal design I moved onto the real design. By breaking my design down into cells it allowed me to make circuit wide changes much easier for optimization of the elements.

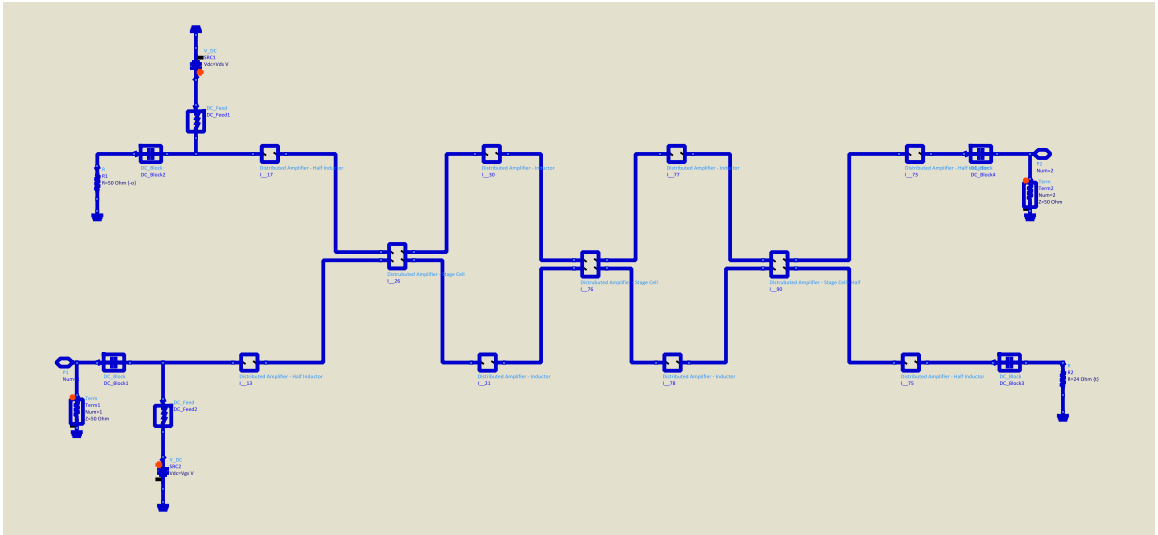


Figure 8: Real design using cells

The Inductor Lg was replaced by a long transmission line (Figure 9) that had similar inductance value as the ideal inductor, and the Cadd was replaced with an extension of line that was placed at the top of the Drain of the transistor (Figure 10).

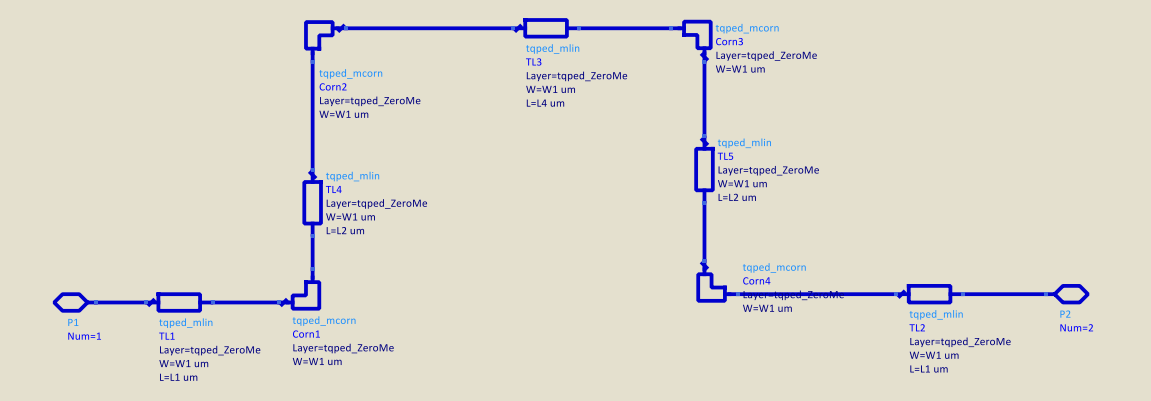


Figure 9: Transmission line similar to Lg

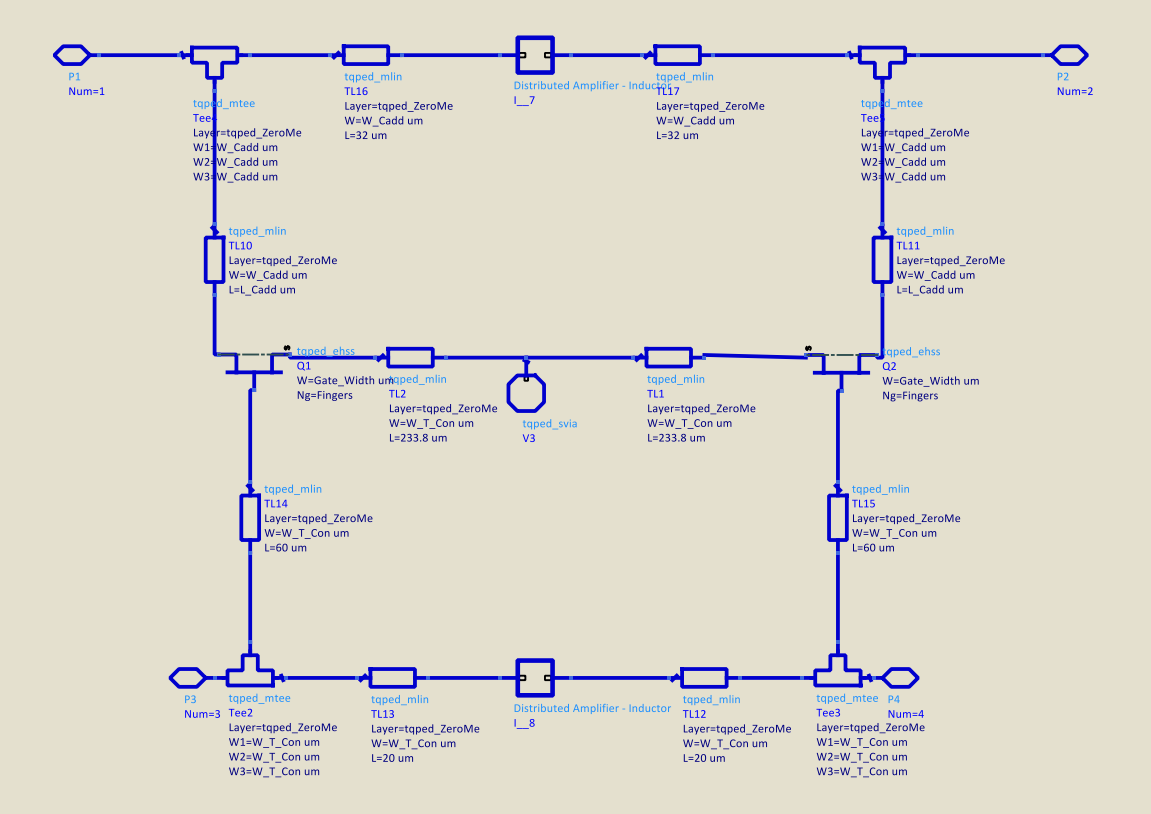


Figure 10: One cell including 2 transistors and one shared

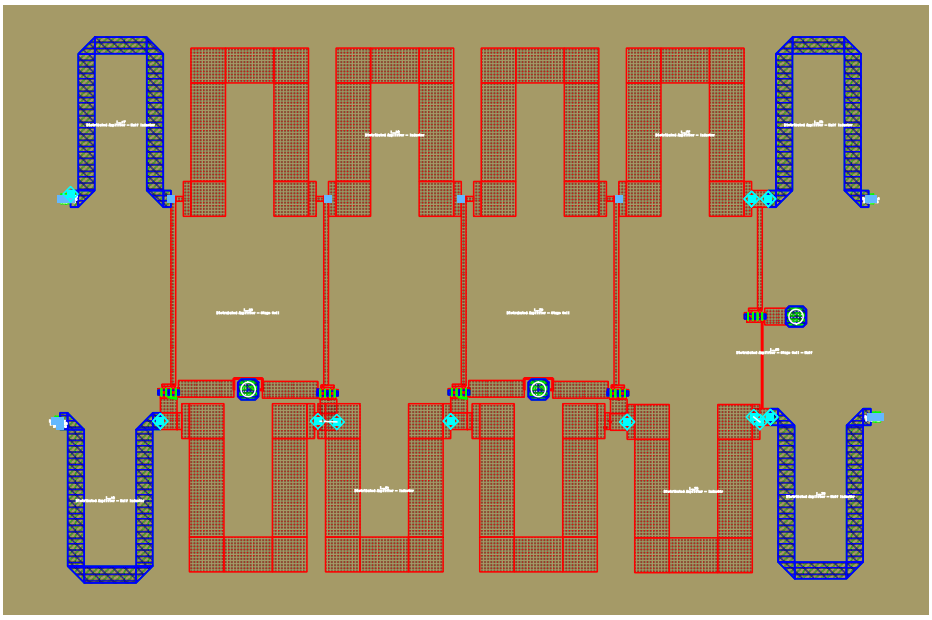


Figure 11: Amplifier layout

Simulation Results

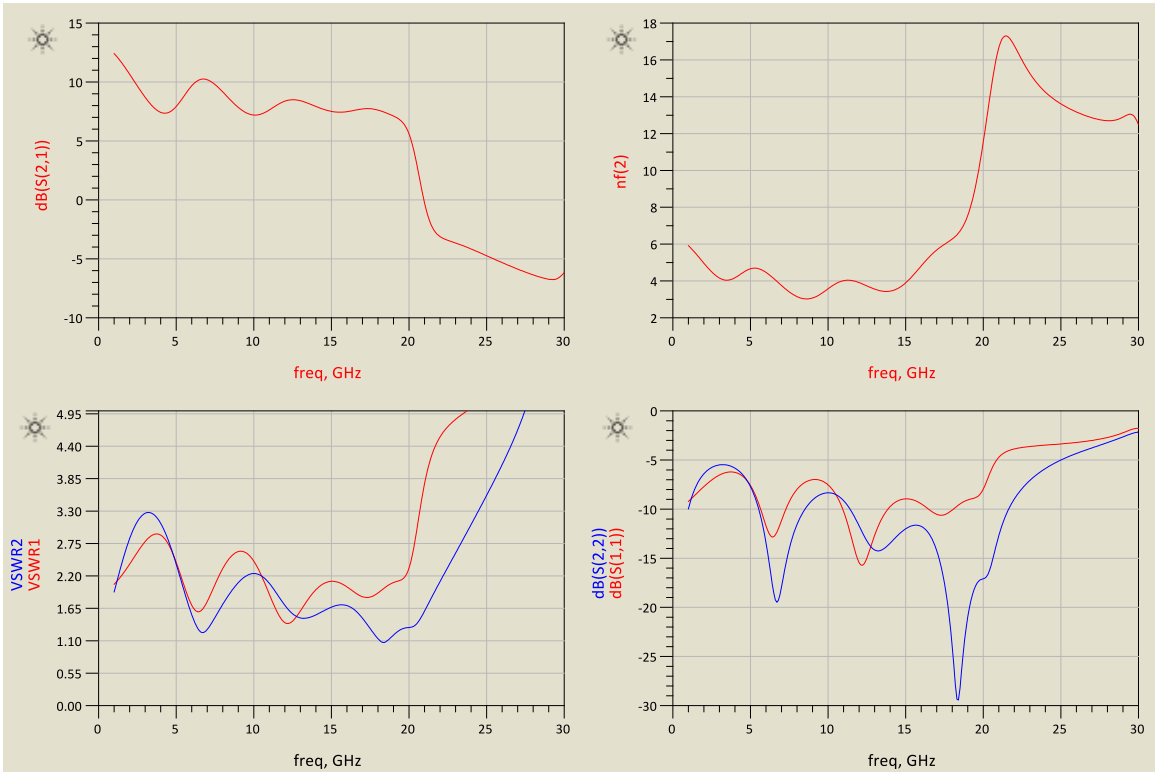


Figure 12: Real amplifier simulation

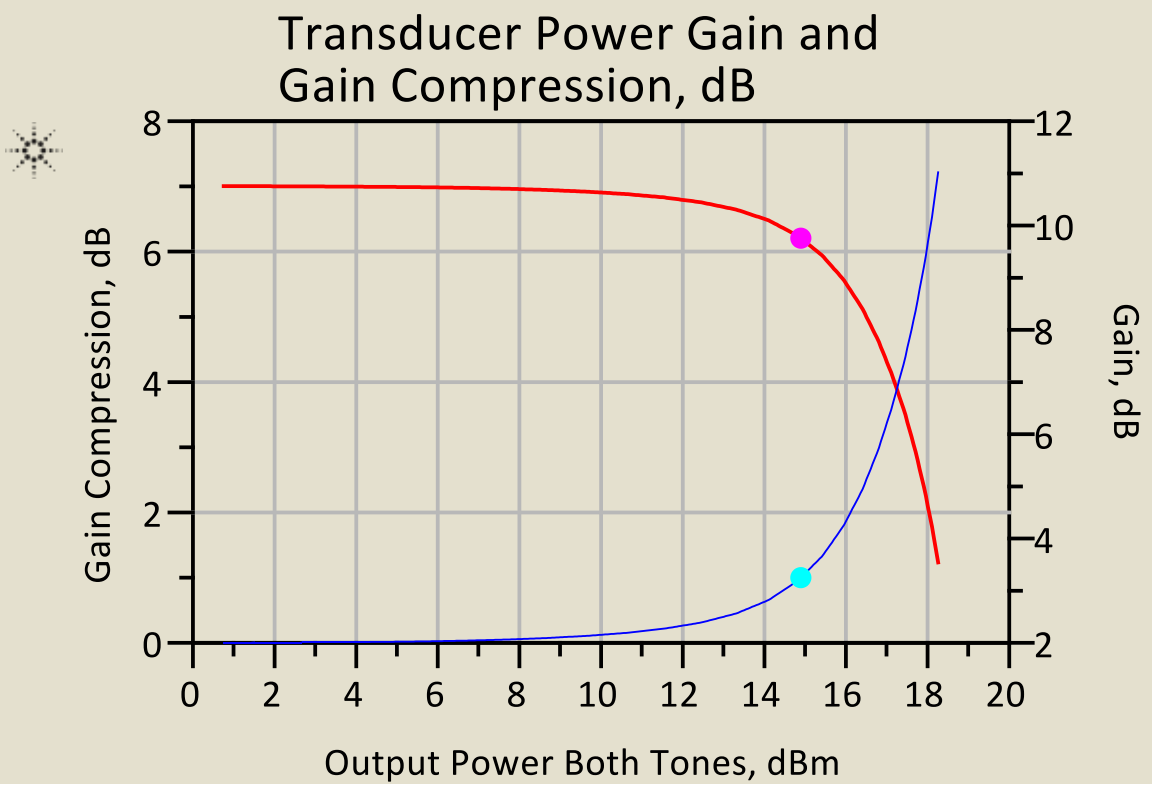


Figure 13: Real Amplifier P1dB

Conclusion

A broadband distributed amplifier was designed and simulated to achieve a decade of bandwidth. The procedure and challenges faced while designing the amplifier were described. Designing an amplifier and meeting all of the required specifications can be realized, but very time consuming. While moving from the ideal to the real design, much work had to be done in order to accommodate for the many parasitics that changed the ideal design once implemented into real components. The P1dB was my primary goal in moving from Ideal to real. Achieving the rest of the design requirements as well as the P1dB proved to be very challenging. In the end I got the P1dB requirement of 15dBm, but the other specifications were not close to the ideal values that I previously simulated.

References

[1] "2014 Monolithic Microwave IC Design Lab G" USF MMIC Design Class